

Claims

What is claimed is:

- 1 1. A mixer circuit for generating an IF output responsive to an RF input and a LO drive  
2 source, comprising:  
3 a mixer core having a doubly balanced mixer including a first differentially coupled  
4 transistor pair and a second differentially coupled transistor pair;  
5 an RF input circuit coupled to the mixer core, the RF input circuit comprising:  
6 an input inductor having a first terminal coupled to receive an RF input signal and  
7 a second terminal;  
8 a biasing resistor having a first terminal coupled to the second terminal of the  
9 input inductor and a second terminal coupled to a first bias voltage;  
10 a first input transistor having a control terminal coupled to the second terminal of  
11 the input inductor, a second terminal, and a third terminal;  
12 a second inductor having a first terminal coupled to the second terminal of the  
13 first input transistor and to the first differentially coupled transistor pair, the second inductor also  
14 having a second terminal coupled to a ground potential;  
15 a supply resistor having a first terminal coupled to the second terminal of the first  
16 input transistor and a second terminal coupled to a supply potential;  
17 a first capacitor having a first terminal also coupled to the second terminal of the  
18 first input transistor and a second terminal coupled to the second differentially coupled  
19 transistor pair; and  
20 a third inductor having a first terminal coupled to the second terminal of the first  
21 capacitor and a second terminal coupled to the ground potential.
- 1 2. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor  
2 pair, the second differentially coupled transistor pair and the first input transistor are all  
3 npn transistors.
- 1 3. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor  
2 pair, the second differentially coupled transistor pair and the first input transistor are all  
3 pnp transistors.
- 1 4. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor  
2 pair, the second differentially coupled transistor pair and the first input transistor are all  
3 MOSFET transistors.

1 5. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor  
2 pair, the second differentially coupled transistor pair and the first input transistor are all  
3 MESFET transistors.

1 6. A mixer circuit for generating an IF output responsive to an RF input and a LO drive  
2 source, comprising:  
3 a mixer core having a doubly balanced mixer including a first differentially coupled npn  
4 transistor pair and a second differentially coupled npn transistor pair, the mixer core coupled to  
5 receive a LO drive signal, the LO drive signal having a plurality of harmonics;  
6 a low noise RF input circuit coupled to the mixer core through a cascode circuit, the low  
7 noise RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further  
8 isolates the RF input circuit from the LO drive signal and the plurality of harmonics.

1 7. A mixer as in Claim 6 wherein the cascode circuit comprises:  
2 a first cascode transistor having an emitter terminal coupled to the second terminal of the  
3 first capacitor and to the first terminal of the third inductor, a collector terminal coupled to the  
4 second differentially coupled npn transistor pair and a base terminal,  
5 a second cascode transistor having a base terminal coupled to the base terminal of the  
6 first cascode transistor, an emitter terminal coupled to the first terminal of the second inductor  
7 and to the emitter terminal of the first npn transistor and a collector terminal coupled to the first  
8 differentially coupled npn transistor pair,  
9 a second capacitor, having a first terminal coupled to the collector terminal of the first  
10 cascode transistor and a second terminal coupled to the base terminal of the first cascode  
11 transistor and to the base terminal of the second cascode transistor,  
12 a third capacitor, having a first terminal coupled to the emitter terminal of the second  
13 cascode transistor and a second terminal coupled to the second terminal of the second capacitor  
14 and to the base terminal of the first cascode transistor and to the base terminal of the first  
15 cascode transistor,  
16 a second biasing resistor having a first terminal coupled to the second terminal of the  
17 third capacitor and a second terminal coupled to a second bias voltage.

1 8. A mixer as in Claim 7, wherein the low noise RF input circuit further includes a RF  
2 feedback circuit, the RF feedback circuit comprising:  
3 a second npn transistor having a base terminal coupled to the supply potential, an  
4 emitter terminal coupled to the collector terminal of the first input npn transistor and a collector  
5 terminal coupled to the first terminal of the supply resistor and to the first terminal of the first  
6 capacitor,  
7 a feedback resistor, having a first terminal coupled to the base terminal of the first  
8 input npn transistor and a second terminal,  
9 a second capacitor, having a first terminal coupled to the second terminal of the  
10 feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

1 9. A mixer as in Claim 7, wherein the mixer core further includes a tracking supply circuit,  
2 the tracking supply circuit comprising:

3 a first diode-connected transistor having a cathode terminal coupled to the ground  
4 potential and an anode terminal,

5 a second diode-connected transistor having a cathode terminal coupled to the  
6 anode terminal of the first diode connected transistor and an anode terminal,

7 a third resistor having a first terminal coupled to the anode terminal of the second  
8 diode connected transistor and a second terminal,

9 a first current supply having a first terminal coupled to the second terminal of the  
10 third resistor and a second terminal coupled to the supply potential,

11 a loop amplifier having a first terminal coupled to the second terminal of the third  
12 resistor and to the first terminal of the first current supply, a second terminal coupled to the  
13 supply potential, a third terminal coupled to the ground potential and a fourth terminal,

14 a fourth resistor having a first terminal coupled to the fourth terminal of the loop  
15 amplifier and a second terminal,

16 a second npn transistor having a collector terminal coupled to the second terminal  
17 of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter  
18 terminal,

19 a third npn transistor having a base terminal coupled to receive a second LO drive  
20 signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a  
21 collector terminal,

22 a fifth resistor having a first terminal coupled to the fourth terminal of the loop  
23 amplifier and a second terminal coupled to the collector terminal of the third npn transistor

24 a second current supply having a first terminal coupled to the emitter terminal of  
25 the second npn transistor and to the emitter terminal of the third npn transistor and a second  
26 terminal coupled to the ground potential,

27 a first common collector amplifier having a base terminal coupled to the second  
28 terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector  
29 terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to  
30 a first mixer core LO input,

31 a third current supply having a first terminal coupled to the emitter terminal of the  
32 first common collector amplifier and a second terminal coupled to the ground potential,

33 a second common collector amplifier having a base terminal coupled to the  
34 second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a  
35 collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal  
36 coupled to a second mixer core LO input,

37 a fourth current supply having a first terminal coupled to the emitter terminal of  
38 the second common collector amplifier and a second terminal coupled to the ground potential.

1 10. A mixer as in Claim 7, wherein the low noise RF input circuit further includes a

2 tracking mixer bias current circuit coupled to the second bias input terminal, the tracking mixer  
3 bias current circuit comprising:  
4 a third resistor having a first terminal coupled to the supply potential and a second  
5 terminal,  
6 a first diode connected transistor having a anode terminal coupled to the second terminal  
7 of the third resistor and a cathode terminal,  
8 a second npn transistor having a collector terminal coupled to the cathode terminal of the  
9 first diode connected transistor, an emitter terminal coupled to the ground potential and a base  
10 terminal,  
11 a loop amplifier having a first terminal coupled to the emitter terminal of the first diode  
12 connected transistor and to the collector terminal of the second npn transistor, a second terminal  
13 coupled to the second bias voltage and a third terminal,  
14 a fourth resistor having a first terminal coupled to the base terminal of the second npn  
15 transistor and a second terminal coupled to the second terminal of the loop amplifier and to the  
16 second bias voltage,  
17 a bandgap voltage supply having a first terminal coupled to the ground potential and a  
18 second terminal coupled to the third terminal of the loop amplifier.

1 11. A mixer circuit as in Claim 6, wherein the mixer core further includes a tracking supply  
2 circuit, the tracking supply circuit comprising:  
3 a first diode-connected transistor having a cathode terminal coupled to the ground  
4 potential and an anode terminal,  
5 a second diode-connected transistor having a cathode terminal coupled to the  
6 anode terminal of the first diode connected transistor and an anode terminal,  
7 a third resistor having a first terminal coupled to the anode terminal of the second  
8 diode connected transistor and a second terminal,  
9 a first current supply having a first terminal coupled to the second terminal of the  
10 third resistor and a second terminal coupled to the supply potential,  
11 a loop amplifier having a first terminal coupled to the second terminal of the third  
12 resistor and to the first terminal of the first current supply, a second terminal coupled to the  
13 supply potential, a third terminal coupled to the ground potential and a fourth terminal,  
14 a fourth resistor having a first terminal coupled to the fourth terminal of the loop  
15 amplifier and a second terminal,  
16 a second npn transistor having a collector terminal coupled to the second terminal  
17 of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter  
18 terminal,  
19 a third npn transistor having a base terminal coupled to receive a second LO drive  
20 signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a  
21 collector terminal,  
22 a fifth resistor having a first terminal coupled to the fourth terminal of the loop  
23 amplifier and a second terminal coupled to the collector terminal of the third npn transistor

24 a second current supply having a first terminal coupled to the emitter terminal of  
25 the second npn transistor and to the emitter terminal of the third npn transistor and a second  
26 terminal coupled to the ground potential,  
27 a first common collector amplifier having a base terminal coupled to the second  
28 terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector  
29 terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to  
30 a first mixer core LO input,  
31 a third current supply having a first terminal coupled to the emitter terminal of the  
32 first common collector amplifier and a second terminal coupled to the ground potential,  
33 a second common collector amplifier having a base terminal coupled to the  
34 second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a  
35 collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal  
36 coupled to a second mixer core LO input,  
37 a fourth current supply having a first terminal coupled to the emitter terminal of  
38 the second common collector amplifier and a second terminal coupled to the ground potential.

1 12. A mixer circuit as in Claim 6, wherein the low noise RF input circuit further includes a  
2 RF feedback circuit coupled to the RF input circuit, the RF feedback circuit comprising:  
3 a second npn transistor having a base terminal coupled to the supply potential, an  
4 emitter terminal coupled to the collector terminal of the first input npn transistor and a collector  
5 terminal coupled to the first terminal of the supply resistor and to the first terminal of the first  
6 capacitor,  
7 a feedback resistor, having a first terminal coupled to the base terminal of the first  
8 input npn transistor and a second terminal,  
9 a second capacitor, having a first terminal coupled to the second terminal of the  
10 feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

1 13. A quadrature mixer circuit for generating a quadrature IF output responsive to an RF  
2 input and a quadrature pair of LO drive signals, comprising:  
3 a mixer core having a first doubly balanced mixer including a first differentially  
4 coupled npn transistor pair and a second differentially coupled npn transistor pair and a second  
5 doubly balanced mixer including a third differentially coupled npn transistor pair and a fourth  
6 differentially coupled npn transistor pair;  
7 an RF input circuit coupled to the mixer core, the RF input circuit comprising:  
8 an input inductor having a first terminal coupled to receive an RF input signal and  
9 a second terminal;  
10 a biasing resistor having a first terminal coupled to the second terminal of the  
11 input inductor and a second terminal coupled to a first bias voltage;  
12 a first input npn transistor having a base terminal coupled to the second terminal  
13 of the input inductor, an emitter terminal, and a collector terminal;  
14 a second inductor having a first terminal coupled to the emitter of the first npn  
15 transistor and to the first differentially coupled npn transistor pair and to the third differentially

16 coupled npn transistor pair, the second inductor also having a second terminal coupled to a  
17 ground potential;  
18 a supply resistor having a first terminal coupled to the collector of the first  
19 transistor and a second terminal coupled to a supply potential;  
20 a first capacitor having a first terminal also coupled to the collector of the first  
21 transistor and a second terminal coupled to the second differentially coupled npn transistor pair  
22 and to the fourth differentially coupled npn transistor pair; and  
23 a third inductor having a first terminal coupled to the second terminal of the first  
24 capacitor and a second terminal coupled to the ground potential.

1 14. A quadrature mixer circuit for generating a quadrature IF output responsive to an RF  
2 input and a quadrature pair of LO drive signals, comprising:  
3 *sub a2* a mixer core having a first doubly balanced mixer including a first differentially coupled  
4 npn transistor pair and a second differentially coupled npn transistor pair and having a second  
5 doubly balanced mixer including a third differentially coupled npn transistor pair and a fourth  
6 differentially coupled npn transistor pair; the mixer core coupled to receive a quadrature LO  
7 drive signal, the quadrature LO drive signal having a plurality of harmonics;  
8 a low noise RF input circuit coupled to the mixer core through a cascode circuit, the low  
9 noise RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further  
10 isolates the RF input circuit from the quadrature LO drive signal and the plurality of harmonics.

1 15. A quadrature mixer as in Claim 14 wherein the cascode circuit comprises:  
2 a first cascode transistor having an emitter terminal coupled to the second terminal of the  
3 first capacitor and to the first terminal of the third inductor, a collector terminal coupled to the  
4 second differentially coupled npn transistor pair and a base terminal,  
5 a second cascode transistor having a base terminal coupled to the base terminal of the  
6 first cascode transistor, an emitter terminal coupled to the first terminal of the second inductor  
7 and to the emitter terminal of the first npn transistor and a collector terminal coupled to the first  
8 differentially coupled npn transistor pair,  
9 a second capacitor, having a first terminal coupled to the collector terminal of the first  
10 cascode transistor and a second terminal coupled to the base terminal of the first cascode  
11 transistor and to the base terminal of the second cascode transistor,  
12 a third capacitor, having a first terminal coupled to the emitter terminal of the second  
13 cascode transistor and a second terminal coupled to the second terminal of the second capacitor  
14 and to the base terminal of the first cascode transistor and to the base terminal of the first  
15 cascode transistor,  
16 a second biasing resistor having a first terminal coupled to the second terminal of the  
17 second capacitor and the first terminal of the third capacitor and a second terminal coupled to a  
18 second bias voltage,  
19 a third biasing resistor having a first terminal coupled to the second bias voltage and to  
20 the second terminal of the second biasing resistor and having a second terminal,

21 a third cascode transistor having a collector terminal coupled to the fourth differentially  
22 coupled npn transistor pair, an emitter terminal coupled to the second terminal of the third  
23 inductor and to the emitter terminal of the first cascode transistor, and a base terminal,  
24 a fourth cascode transistor having a base terminal coupled to the base terminal of the  
25 third cascode transistor, a collector terminal coupled the third differentially coupled npn  
26 transistor pair and an emitter terminal coupled to the emitter terminal of the second cascode  
27 transistor and to the second terminal of the second inductor,  
28 a fourth capacitor having a first terminal coupled to the emitter terminal of the third  
29 cascode transistor and a second terminal coupled to the base terminal of the third and fourth  
30 cascode transistors,  
31 a fifth capacitor having a first terminal coupled to the second terminal of the fourth  
32 capacitor and to the base terminals of the third and fourth cascode transistors and a second  
33 terminal coupled to the emitter terminal of the fourth cascode transistor.

1 16. A quadrature mixer as in Claim 15 wherein the low noise RF input circuit further  
2 includes a RF feedback circuit, the RF feedback circuit comprising:  
3 a second npn transistor having a base terminal coupled to the supply  
4 potential, an emitter terminal coupled to the collector terminal of the first input npn transistor  
5 and a collector terminal coupled to the first terminal of the supply resistor and to the first  
6 terminal of the first capacitor,  
7 a feedback resistor, having a first terminal coupled to the base terminal of  
8 the first input npn transistor and a second terminal,  
9 a sixth capacitor, having a first terminal coupled to the second terminal of  
10 the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

1 17. A quadrature mixer as in Claim 16, wherein the mixer core further includes a first  
2 tracking supply circuit portion coupled to the In-Phase LO drive input terminals of the  
3 mixer core and a second tracking supply circuit portion coupled to the Quadrature Phase  
4 LO drive input terminals of the mixer core.

1 18. A mixer circuit as in Claim 17, wherein the first tracking supply comprises:  
2 a. a first diode-connected transistor having a cathode terminal coupled to the ground  
3 potential and an anode terminal;  
4 b. a second diode-connected transistor having a cathode terminal coupled to the  
5 anode terminal of the first diode connected transistor and an anode terminal,  
6 c. a third resistor having a first terminal coupled to the anode terminal of the second  
7 diode connected transistor and a second terminal;  
8 d. a first current supply having a first terminal coupled to the second terminal of the  
9 third resistor and a second terminal coupled to the supply potential;  
10 e. a loop amplifier having a first terminal coupled to the second terminal of the third  
11 resistor and to the first terminal of the first current supply, a second terminal

- 12 coupled to the supply potential, a third terminal coupled to the ground potential  
13 and a fourth terminal;
- 14 f. a fourth resistor having a first terminal coupled to the fourth terminal of the loop  
15 amplifier and a second terminal;
- 16 g. a second npn transistor having a collector terminal coupled to the second terminal  
17 of the fourth resistor, a base terminal coupled to receive a first LO drive signal  
18 and emitter terminal;
- 19 h. a third npn transistor having a base terminal coupled to receive a second LO drive  
20 signal, an emitter terminal coupled to the emitter terminal of the second npn  
21 transistor and a collector terminal;
- 22 i. a fifth resistor having a first terminal coupled to the fourth terminal of the loop  
23 amplifier and a second terminal coupled to the collector terminal of the third npn  
24 transistor;
- 25 j. a second current supply having a first terminal coupled to the emitter terminal of  
26 the second npn transistor and to the emitter terminal of the third npn transistor  
27 and a second terminal coupled to the ground potential;
- 28 k. a first common collector amplifier having a base terminal coupled to the second  
29 terminal of the fifth resistor and to the collector terminal of the third npn  
30 transistor, a collector terminal coupled to the fourth terminal of the loop  
31 amplifier, and an emitter terminal coupled to a first mixer core LO input;
- 32 l. a third current supply having a first terminal coupled to the emitter terminal of the  
33 first common collector amplifier and a second terminal coupled to the ground  
34 potential;
- 35 m. a second common collector amplifier having a base terminal coupled to the  
36 second terminal of the fourth resistor and to the collector terminal of the second  
37 npn transistor, a collector terminal coupled to the fourth terminal of the loop  
38 amplifier and an emitter terminal coupled to a second mixer core LO input; and
- 39 n. a fourth current supply having a first terminal coupled to the emitter terminal of  
40 the second common collector amplifier and a second terminal coupled to the  
41 ground potential;
- 42 and wherein the second tracking supply circuit portion comprises:
- 43 o. a third diode-connected transistor having a cathode terminal coupled to the  
44 ground potential and an anode terminal;
- 45 p. a fourth diode-connected transistor having a cathode terminal coupled to the  
46 anode terminal of the third diode connected transistor and an anode terminal;
- 47 q. a third resistor having a first terminal coupled to the anode terminal of the second  
48 diode connected transistor and a second terminal;
- 49 r. a first current supply having a first terminal coupled to the second terminal of the  
50 third resistor and a second terminal coupled to the supply potential;
- 51 s. a loop amplifier having a first terminal coupled to the second terminal of the third  
52 resistor and to the first terminal of the first current supply, a second terminal  
53 coupled to the supply potential, a third terminal coupled to the ground potential  
54 and a fourth terminal;



- t. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;
- u. a second npn transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal;
- v. a third npn transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a collector terminal;
- w. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third npn transistor;
- x. a second current supply having a first terminal coupled to the emitter terminal of the second npn transistor and to the emitter terminal of the third npn transistor and a second terminal coupled to the ground potential;
- y. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;
- z. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;
- aa. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input;
- bb. a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

19. A quadrature mixer as in Claim 15, wherein the low noise RF input circuit further includes a tracking mixer bias current circuit, the tracking bias current circuit comprising:
- a first resistor having a first terminal coupled to the supply potential and a second terminal,
  - a first diode connected transistor having a anode terminal coupled to the second terminal of the third resistor and a cathode terminal,
  - a second npn transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,
  - a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second npn transistor, a second terminal coupled to the second bias voltage and a third terminal,

14 a second resistor having a first terminal coupled to the base terminal of the second  
15 npn transistor and a second terminal coupled to the second terminal of the loop amplifier and to  
16 the second bias voltage,  
17 a bandgap voltage supply having a first terminal coupled to the ground potential  
18 and a second terminal coupled to the third terminal of the loop amplifier.

1 20. A mixer circuit for generating an IF output responsive to an RF input and a LO drive  
2 source, comprising:  
3 a mixer core having a doubly balanced mixer including a first differentially coupled npn  
4 transistor pair and a second differentially coupled npn transistor pair;  
5 a single ended RF input circuit coupled to receive an RF signal, the RF circuit coupled to  
6 the mixer core, the RF circuit including means for providing an input impedance, means for  
7 splitting a phase of the RF signal, and means for decoupling noise from the RF signal to the  
8 mixer core.

1 21. A mixer circuit for generating an IF output responsive to an RF input and a LO drive  
2 source, comprising:  
3 a mixer core having a doubly balanced mixer including a first differentially coupled npn  
4 transistor pair and a second differentially coupled npn transistor pair, the mixer core coupled to  
5 receive a LO drive signal, the LO drive signal having a plurality of harmonics;  
6 a low noise single ended RF input circuit coupled to the mixer core through a cascode  
7 circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the cascode  
8 circuit further isolates the RF input circuit from the LO drive signal and the plurality of  
9 harmonics the RF circuit including means for providing an input impedance and means for  
10 splitting a phase of the RF signal.